SONY

CXB1582Q

Fibre Channel Receiver

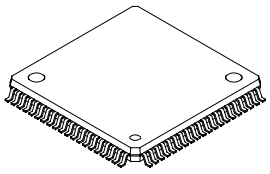
Description

The CXB1582Q is a receiver IC with a built-in PLL clock recovery circuit for high-speed serial data reception. It can be used together with the transmitter IC CXB1581Q as a chip set, and 1062.5Mbaud, 20-bit or 531.25Mbaud, 10-bit operation can be selected.

Features

- Conforms to ANSI X3T11 Fibre channel standard
- Supports GLM (Gigabaud Link Module) interface
- Built-in low-jitter PLL clock recovery circuit
- Single 3.3V power supply or dual 3.3V/5V power supply (for 5V TTL interface) operation can be selected.
- Low power consumption: 910mW (Typ.) when operating with a single 3.3V power supply
- 1062.5Mbaud, 20-bit or 531.25Mbaud, 10-bit operation can be selected.
- PLL lock detection circuit
- Power-on reset signal output circuit

80 pin QFP (Plastic)



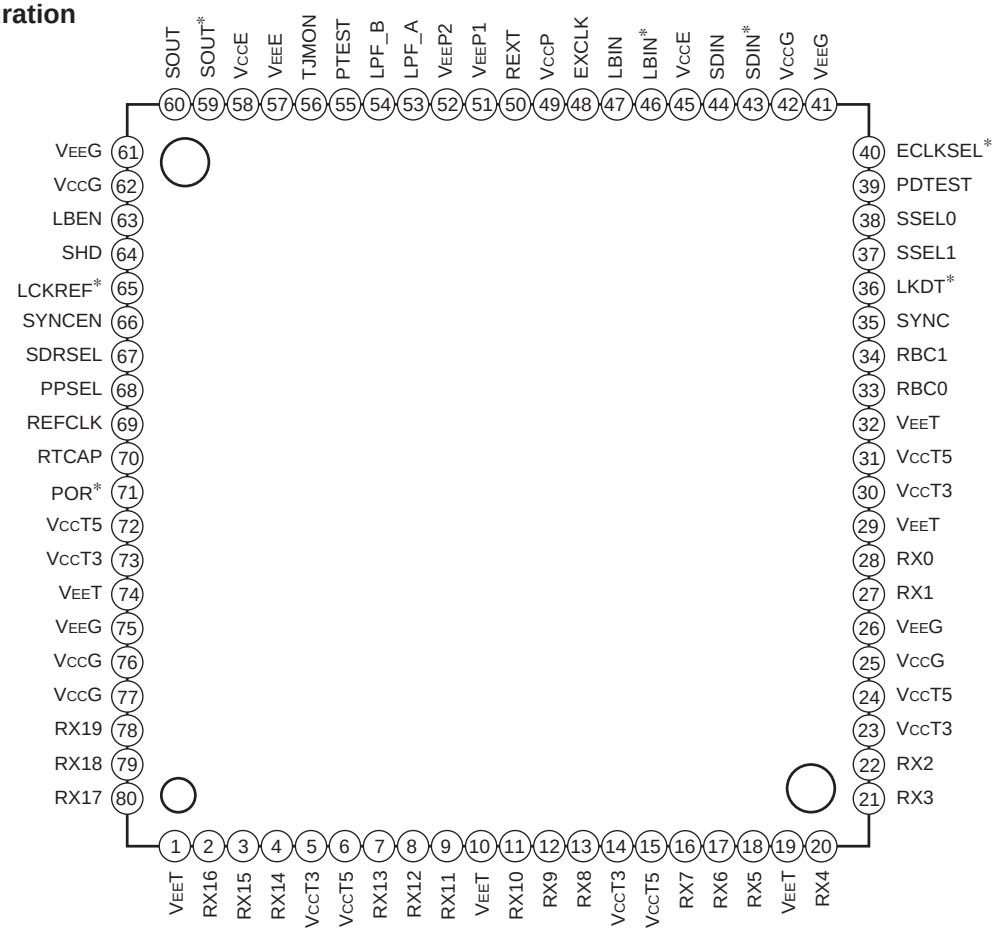
Applications

Fibre channel 1062.5Mbaud and 531.25Mbaud communications

Structure

Bipolar silicon monolithic IC

Pin Configuration



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E95930-ST

Absolute Maximum Ratings ($V_{EE}E$, $V_{EE}T$, $V_{EE}G$, $V_{EE}P$ = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (excluding $V_{CC}T5$)	V_{CC}	–0.3		4	V
Supply voltage for TTL output	$V_{CC}T5$	$V_{CC}G$ – 2, or –0.3		$V_{CC}G$ + 5, or 5.5	V
TTL DC input voltage	V_I_T	–0.5		5.5	V
ECL DC input voltage	V_I_E	V_{CC} – 2		V_{CC}	V
ECL differential input voltage	V_{IS}_E	–2		2	V
TTL output current (High level)	I_{OH}_T	–20		0	mA
TTL output current (Low level)	I_{OL}_T	0		20	mA
ECL output current	I_O_E	–30		0	mA
Operating ambient temperature	Ta	–55		70	°C
Storage temperature	Tstg	–65		150	°C

Recommended Operating Conditions ($V_{EE}E$, $V_{EE}T$, $V_{EE}G$, $V_{EE}P$ = 0V)

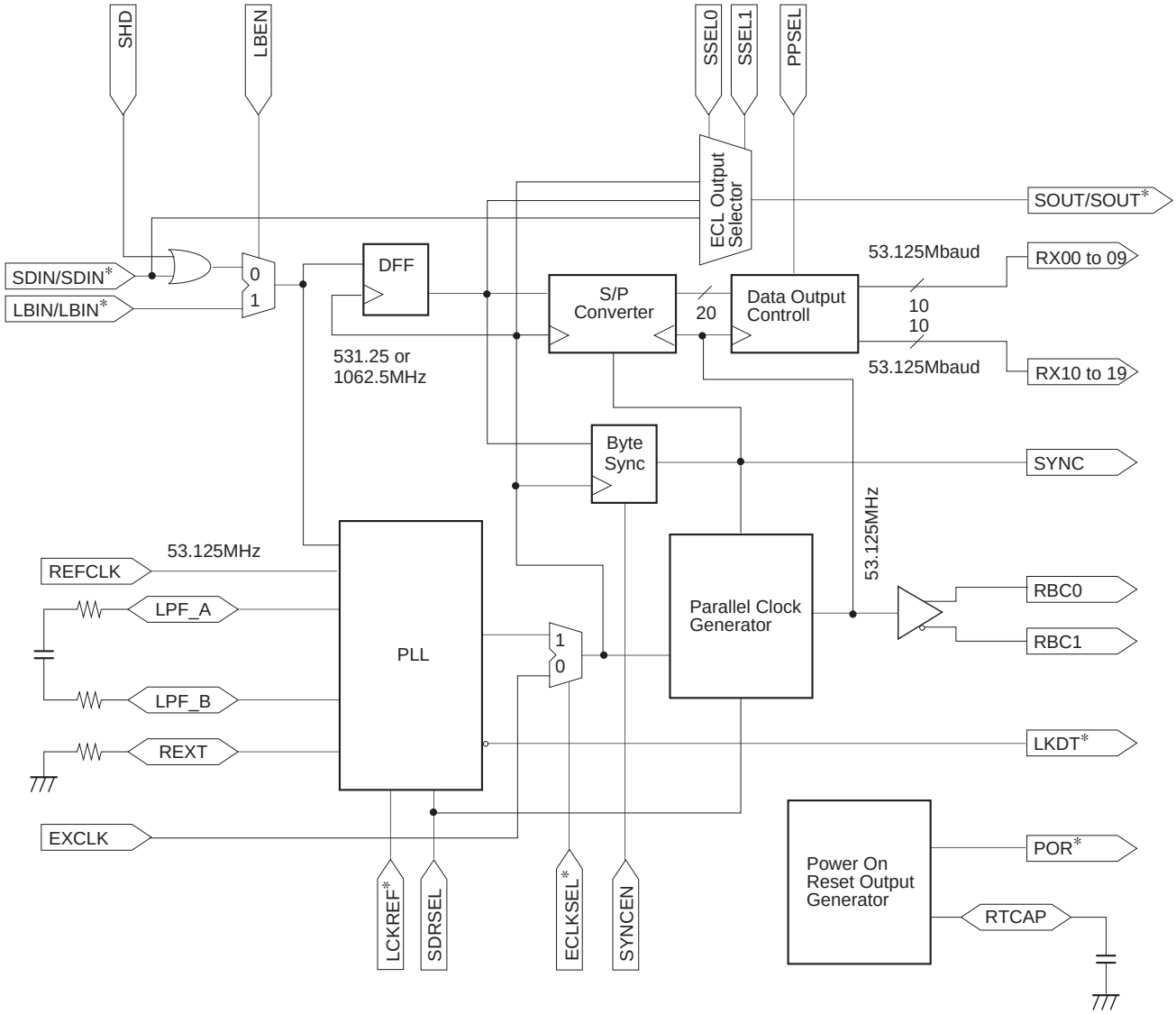
During single 3.3V power supply operation

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (including $V_{CC}T5$)	V_{CC}	3.135	3.3	3.465	V
Ambient temperature	Ta	0		70	°C

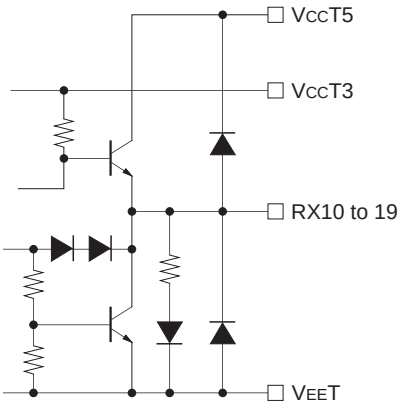
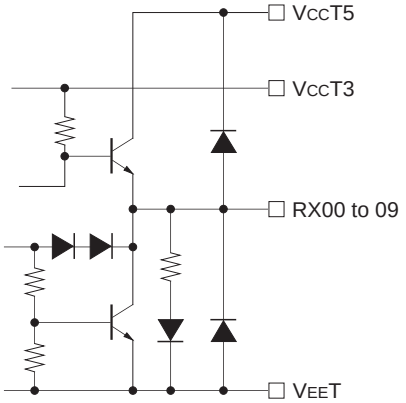
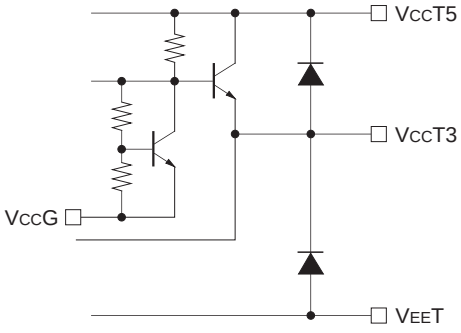
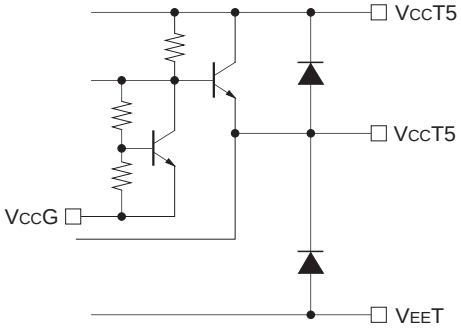
During dual 3.3V/5V power supply operation ($V_{CC}T3$ open)

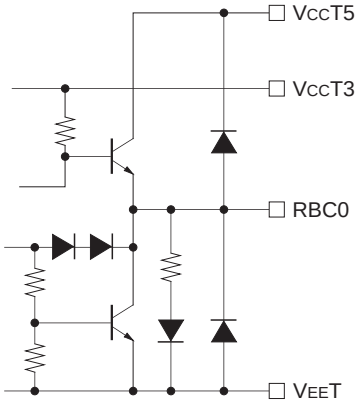
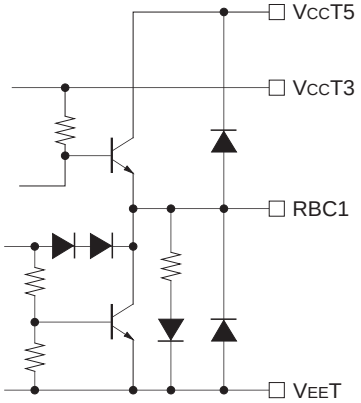
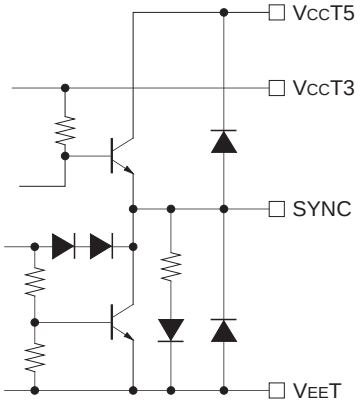
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (excluding $V_{CC}T5$)	V_{CC}	3.135	3.3	3.465	V
Power supply for TTL output	$V_{CC}T5$	4.75	5	5.25	V
Ambient temperature	Ta	0		70	°C

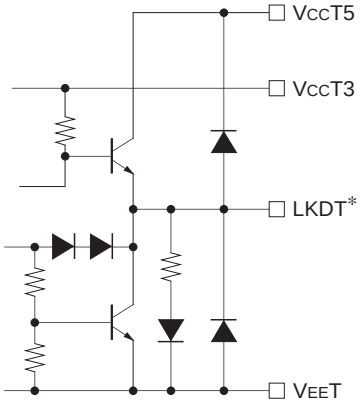
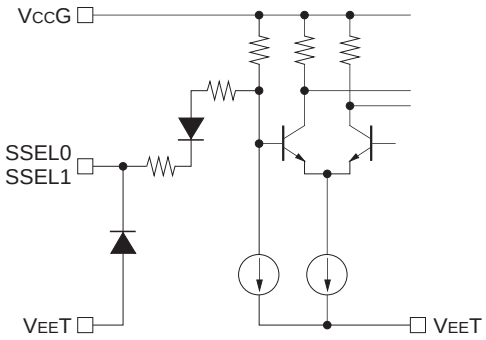
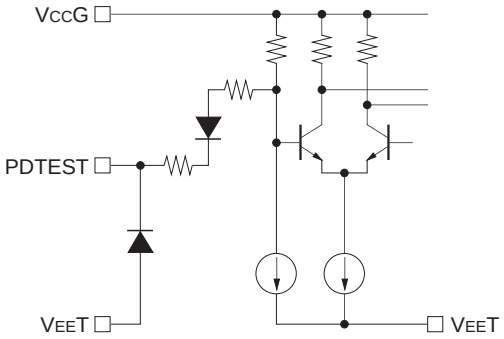
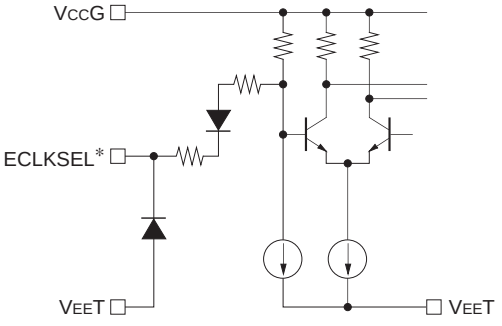
Block Diagram

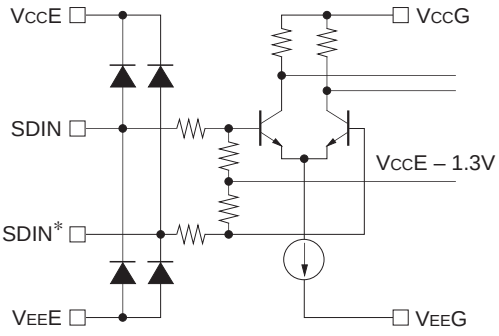
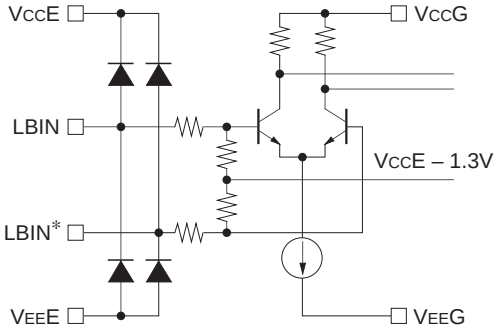
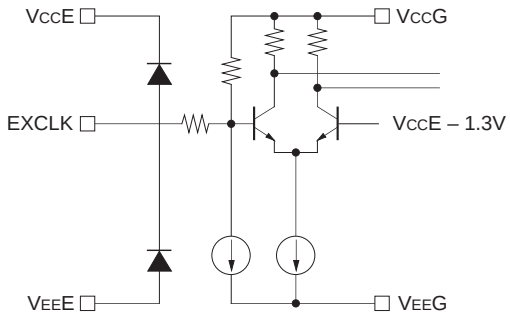
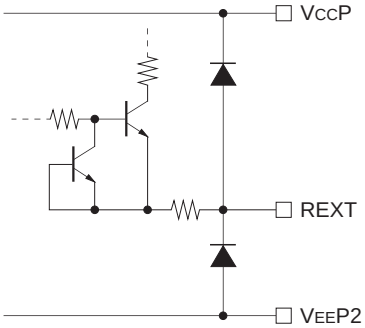


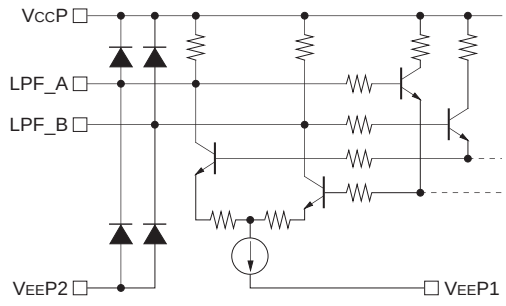
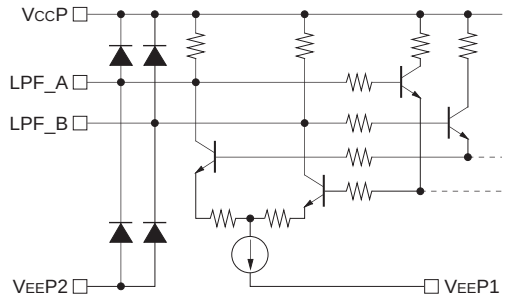
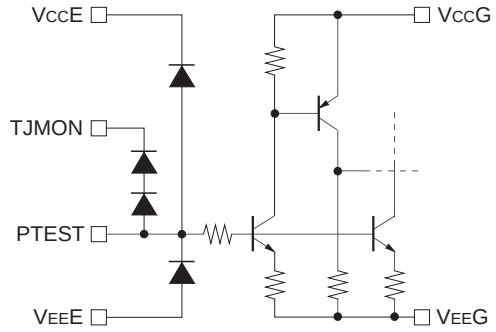
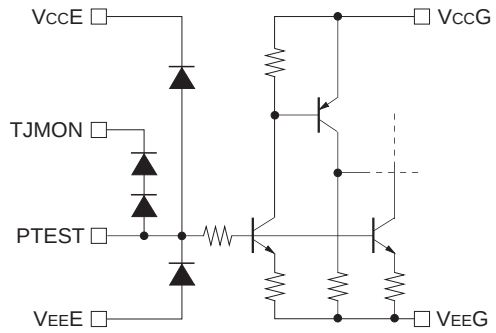
Pin Description

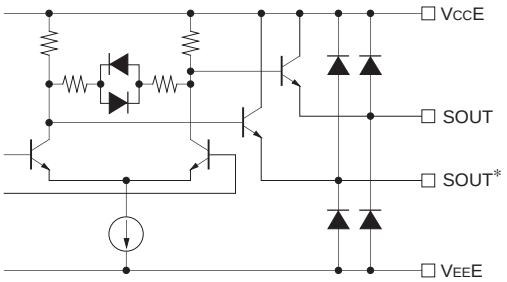
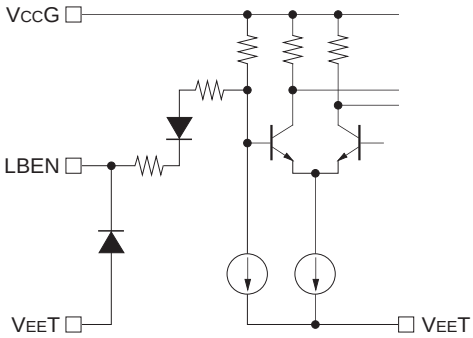
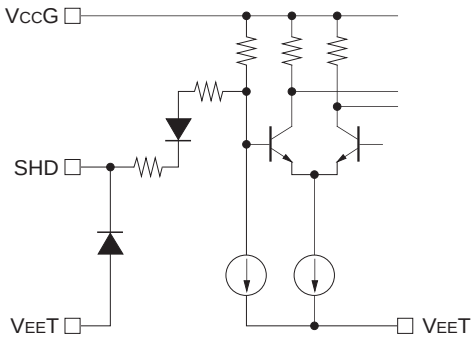
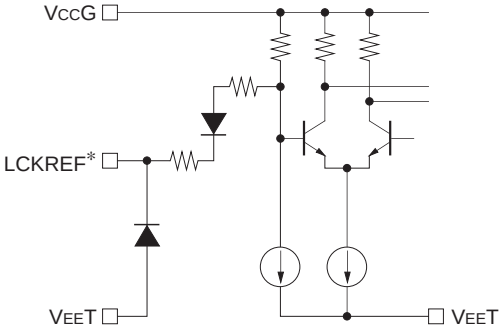
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
1, 10, 19, 29, 32, 74	$V_{EE}T$	Power supply	0V	—	Negative power supplies for TTL output.
78 to 80, 2 to 4, 7 to 9, 11	RX19 to RX17, RX16 to RX14, RX13 to RX11, RX10	TTL output	TTL level		Parallel data outputs (Byte_1).
12, 13, 16 to 18, 20 to 22, 27, 28	RX09, RX08, RX07 to RX05, RX04 to RX02, RX01, RX00	TTL output	TTL level		Parallel data outputs (Byte_0). The first data of the serial data is RX00 and the last data is RX19 (RX09 during 531Mbaud mode).
5, 14, 23, 30 73	$V_{CC}T3$	Power supply	3.3V or open		Positive power supply for TTL output. Set to 3.3V when using the IC with a single 3.3V power supply; leave open when using the IC with a dual 3.3V/5V power supply.
6, 15, 24, 31 72	$V_{CC}T5$	Power supply	3.3V or 5V		Positive power supply for TTL output. Set to 3.3V when using the IC with a single 3.3V power supply; to 5V when using the IC with a dual 3.3V/5V power supply.

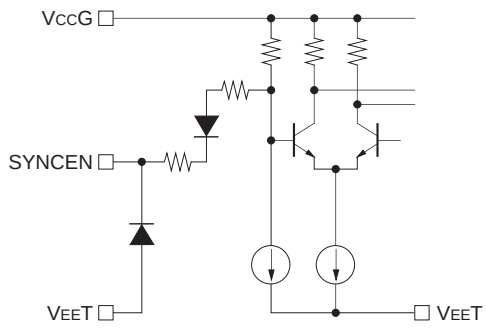
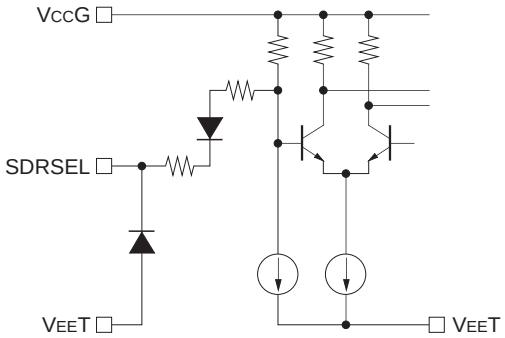
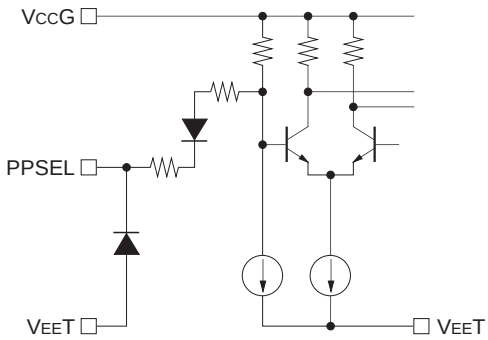
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
25, 42, 62, 76, 77	$V_{CC}G$	Power supply	3.3V	—	Positive power supplies for internal logic gate.
26, 41, 61, 75	$V_{EE}G$	Power supply	0V	—	Negative power supplies for internal logic gate.
33	RBC0	TTL output	TTL level		Receive byte clock 0 output. This clock is used when loading parallel data (RX00 to RX19) using the system in the next stage.
34	RBC1	TTL output	TTL level		Receive byte clock 1 output. Inverse of the RBC0 clock.
35	SYNC	TTL output	TTL level		Byte sync output. This pin outputs high level when +Comma (0011111) or –Comma (1100000) is detected in the serial data. (See the Timing Charts.)

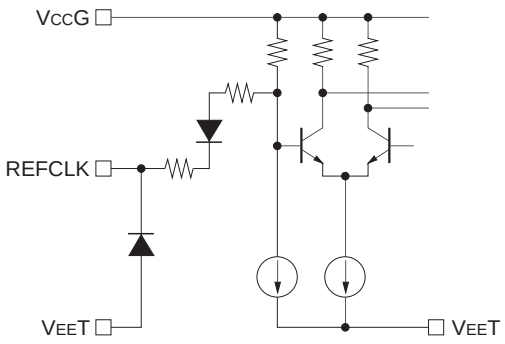
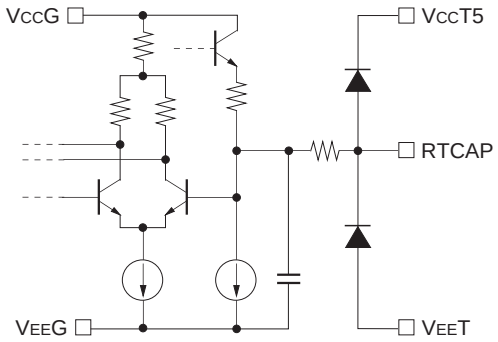
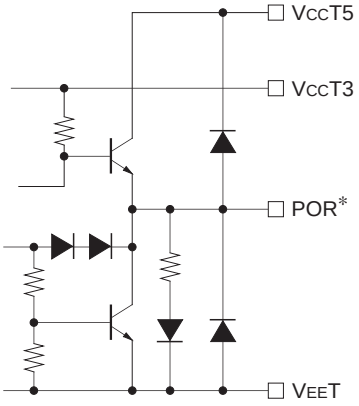
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
36	LKDT*	TTL output	TTL level		PLL lock detection signal output. This pin outputs low level when the PLL is locked to the serial data and high level when the PLL becomes unlocked.
37 38	SSEL1 SSEL0	TTL input	TTL level		SOUT/SOUT* output signal selection. (See Table 1.)
39	PDTEST	TTL input	0V		Test. Connect to VeeG.
40	ECLKSEL*	TTL input	TTL high level or 3.3V		External clock selection. When this pin is set to low level, the clock input to EXCLK is used as the bit rate clock.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
43 44	SDIN* SDIN	ECL input (differen-tial)	ECL level		Serial data inputs. These input pins are enabled when SHD is set to low level.
45, 58	VCCE	Power supply	3.3V	—	Positive power supplies for ECL I/O.
46 47	LBIN* LBIN	ECL input (differen-tial)	ECL level		Serial data inputs for loop-back test. These input pins are enabled when LBEN is set to high level.
48	EXCLK	ECL input	ECL level		External clock input. When ECLKSEL* is set to low level, the clock input to this pin is used as the bit rate clock. This pin is biased to become low level when left open.
49	VCCP	Power supply	3.3V	—	Positive power supply for internal PLL.
50	REXT	External part connec-tion pin	—		Connects the resistor which determines the VCO center frequency. Connect a 4.7kΩ resistor between this pin and VEEP1. (See Notes on Operation and Fig. 1.)
51	VEEP1	Power supply	0V	—	Negative power supply for internal PLL.
52	VEEP2	Power supply	0V	—	Negative power supply for internal PLL.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
53	LPF_A	External part connec-tion pin	—		External loop filter connection. (See Notes on Operation and Fig. 1.)
54	LPF_B	External part connec-tion pin	—		External loop filter connection. (See Notes on Operation and Fig. 1.)
55	PTEST	TTL input	0V		Test. Connect to VEEP1.
56	TJMON	Test pin	0V		Junction temperature measurement. Connect to VEEP.
57	VEEE	Power supply	0V	—	Negative power supply for ECL I/O.

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
59 60	SOUT* SOUT	ECL output (differen-tial)	ECL level		High-speed signal monitor. The monitored signal can be selected with SSEL0/1. (See Table 1.)
63	LBEN	TTL input	TTL level		Loop-back enable. When this pin is set to high level, LBIN functions as a serial data input.
64	SHD	TTL input	TTL level		Serial data input shutdown. When this pin is set to high level, the serial data is fixed to low level regardless of the signal input to SDIN.
65	LCKREF*	TTL input	TTL level		Lock-to-reference signal input. Setting this pin to low level forcibly locks the PLL to REFCLK.

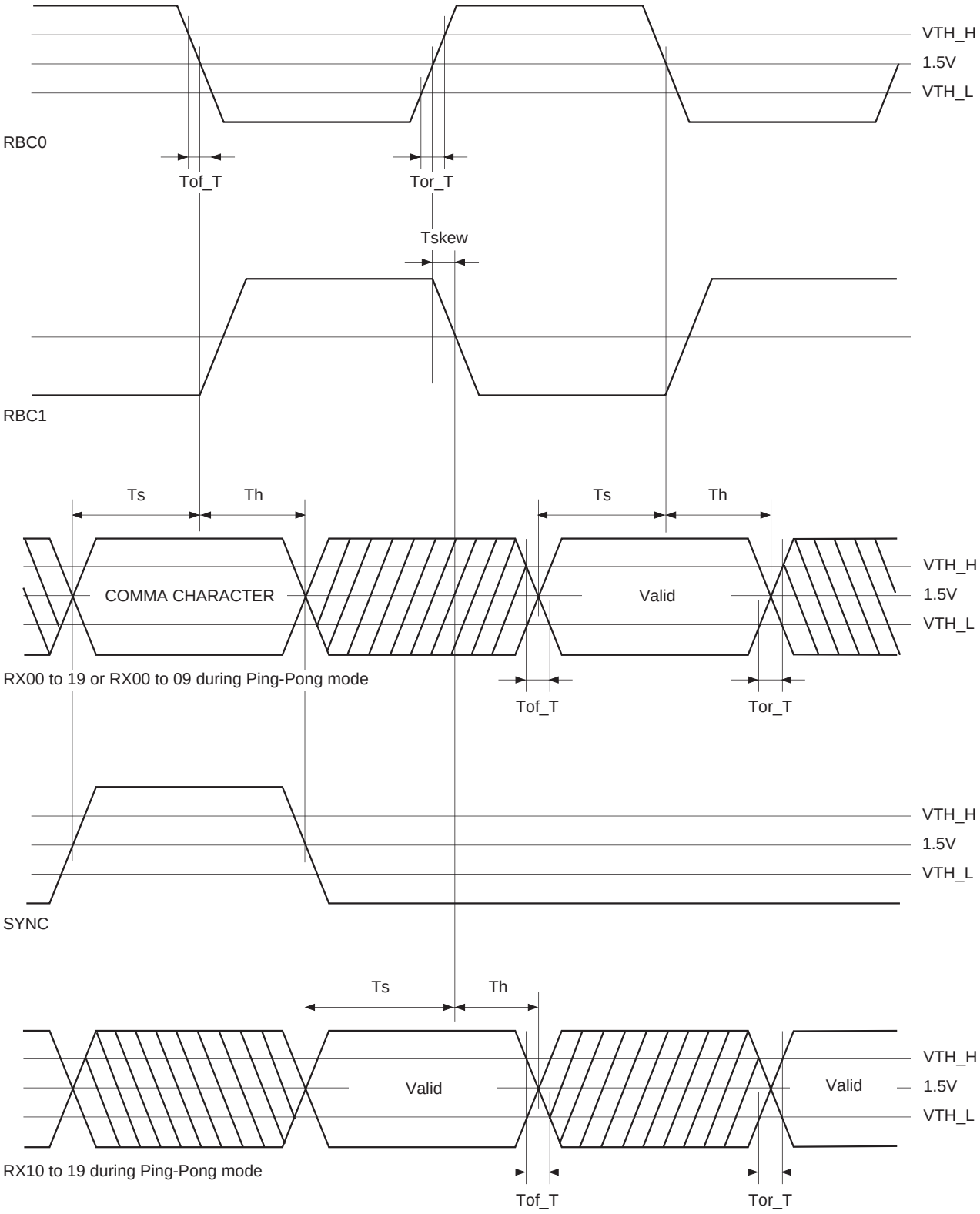
Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
66	SYNCEN	TTL input	TTL level		Byte sync enable signal input. When this pin is set to high level, +Comma (0011111) or –Comma (1100000) is detected and the parallel data is synchronized to this byte. (See the Timing Charts.) When this pin is set to low level, byte synchronization is not performed.
67	SDRSEL	TTL input	TTL level		Serial data rate selection. Setting this pin to low level selects 531.25Mbaud mode and to high level selects 1.0625Gbaud mode.
68	PPSEL	TTL input	TTL level		Ping-Pong mode selection. When this signal is set to high level during 1.0625Gbaud mode (SDRSEL = high), parallel data is output during Ping-Pong mode. In other words, byte 0 is output in sync with the rise of RBC0, and byte 1 with the rise of RBC1. (See the Timing Charts.)

Pin No.	Symbol	Type	Typical pin I/O voltage	Equivalent circuit	Description
69	REFCLK	TTL input	TTL level		Reference clock input. This pin is used for PLL frequency pull-in. Input the clock with 1/20 frequency of the serial data rate during 1.0625Gbaud mode or with 1/10 frequency of the serial data rate during 531.25Mbaud mode (around 53.125MHz in either case).
70	RTCAP	External part connec-tion pin	—		Connects the capacitor which determines the POR* (power-on reset signal) low time. (See Notes on Operation and Fig. 4.)
71	POR*	TTL output	TTL level		Power-on reset signal output. When the power is turned on, POR* maintains low level for approximately 100ns and then goes to high level. (See Notes on Operation and Fig. 4.)

SSEL0	SSEL1	SOUT/SOUT*
0	0	Non Retimed Serial Data.
1	0	Retimed Serial Data.
0	1	Recovered Bit Rate Clock
1	1	Testing output. Fixed to low.

Table 1. Monitor Output (SOUT) Selection Table

Timing Charts



During single 3.3V power supply operation: VTH_L = 0.8V, VTH_H = 2.0V
During dual 3.3V/5.0V power supply operation: VTH_L = 0.6V, VTH_H = 2.2V

Electrical Characteristics

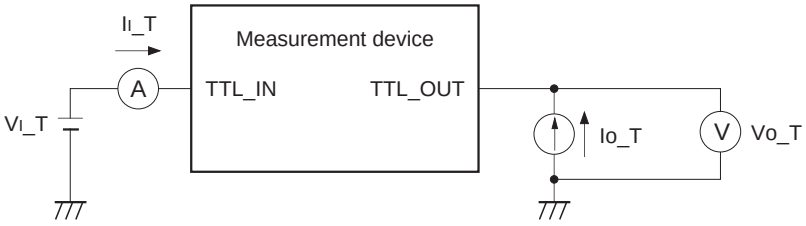
DC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
TTL high level input voltage	V_{IH}_T	2		5.5	V	
TTL low level input voltage	V_{IL}_T	0		0.8	V	
TTL high level input current	I_{IH}_T			20	µA	$V_{IH} = V_{CC}$
TTL low level input current	I_{IL}_T	–400			µA	$V_{IL} = 0$
TTL high level output voltage	V_{OH}-T					
Single 3.3V power supply		2.2			V	I_{OH} = –0.4mA
Dual 3.3V/5V power supply		2.6			V	I_{OH} = –0.4mA
TTL low level output voltage	V_{OL}_T					
Single 3.3V power supply				0.5	V	I_{OL} = 2mA
Dual 3.3V/5V power supply				0.5	V	I_{OL} = 4mA
ECL high level input voltage	V_{IH}_E	V_{CC} – 1.17		V_{CC} – 0.88	V	
ECL low level input voltage	V_{IL}_E	V_{CC} – 1.81		V_{CC} – 1.48	V	
ECL differential input voltage	V_{IS}_E	200		1000	mV	AC coupling input
ECL high level output voltage	V_{OH}_E	V_{CC} – 1.05		V_{CC} – 0.81	V	50Ω terminated to V_{CC} – 2V
ECL low level output voltage	V_{OL}_E	V_{CC} – 1.81		V_{CC} – 1.55	V	50Ω terminated to V_{CC} – 2V
ECL output amplitude	V_{OS}_E	650			mV	50Ω terminated to V_{CC} – 2V
Current consumption	I_{CC}					Output pins open
Single 3.3V power supply			274	343	mA	
Dual 3.3V/5V power supply			182 99	228 124	mA mA	3.3V power supply 5V power supply (V_{CC}T5)
Power consumption	P_D					Output pins open
Single 3.3V power supply			0.91	1.19	W	
Dual 3.3V/5V power supply			1.10	1.44	W	

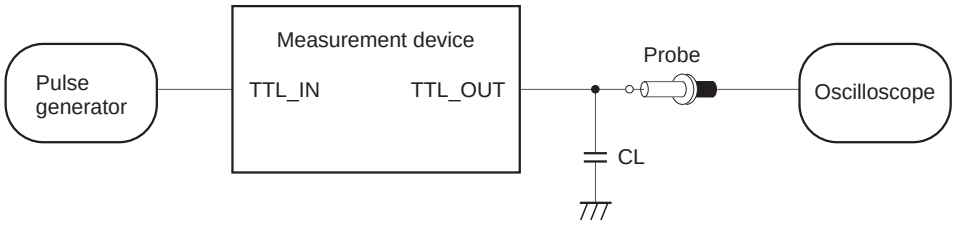
AC Characteristics (under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
REFCLK rise time	Tir_RC			4.8	ns	0.8 to 2.0V
REFCLK fall time	Tif_RC			4.8	ns	2.0 to 0.8V
TTL output rise time	Tor_T					
Single 3.3V power supply				3.5	ns	0.8 to 2.0V, CL = 10pF
Dual 3.3V/5V power supply				3.2	ns	0.6 to 2.2V, CL = 10pF
TTL output fall time	Tof_T					
Single 3.3V power supply				3.5	ns	2.0 to 0.8V, CL = 10pF
Dual 3.3V/5V power supply				3.2	ns	2.2 to 0.6V, CL = 10pF
ECL output rise time	Tor_E			400	ps	20 to 80%, CL ≤ 2pF
ECL output fall time	Tof_E			400	ps	20 to 80%, CL ≤ 2pF
SDIN data rate	R_SDIN					
531.25Mbaud mode		500	531.25	550	Mbaud	
1062.5Mbaud mode		1000	1062.5	1100	Mbaud	
REFCLK cycle tolerance	Ttol_RC	–100	0	100	ppm	Using the SDIN cycle as a reference
RBC0/1 skew	Tskew	–1		1	ns	
RBC duty cycle	DC_RBC	40		60	%	
RX setup time	Ts	3			ns	RBC reference
RX hold time	Th	7.53			ns	RBC reference
Jitter tolerance	JT			0.7	UI	
Bit sync time	Tbs			2500	bit	FC Idle Pattern
Frequency acquisition time	Tfa			500	µs	Loop Damping Capacitor C1 = 0.01µF

Electrical Characteristics Measurement Circuit (See Fig. 3 Power Supply Circuits regarding the power supply.)

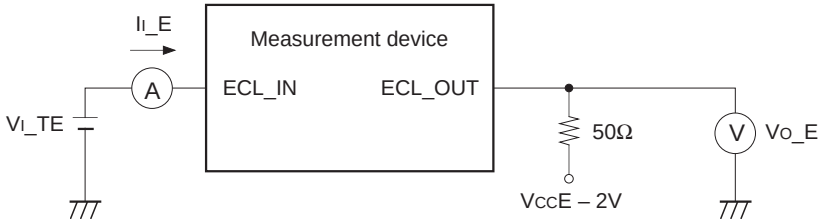


(a) TTL I/O DC characteristics measurement circuit

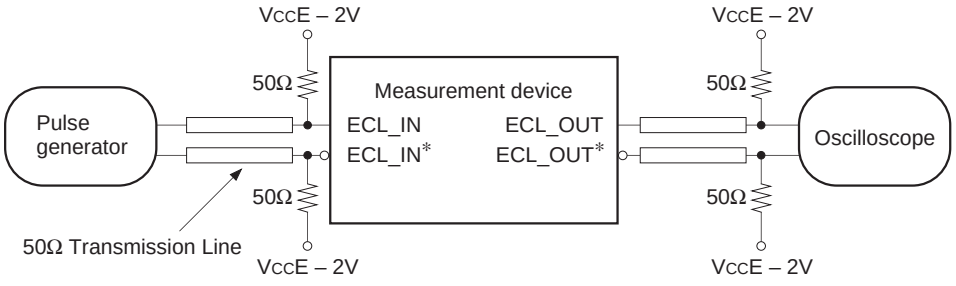


CL = 10pF (including the probe capacitance)

(b) TTL I/O AC characteristics measurement circuit

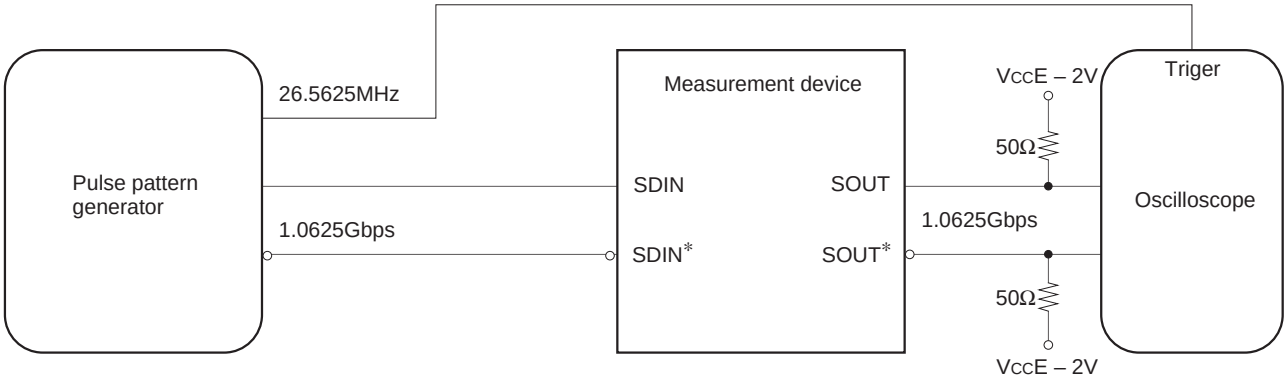


(c) ECL I/O DC characteristics measurement circuit



CL ≤ 2pF (input capacitance of the measurement instrument and floating capacitance)

(d) ECL I/O AC characteristics measurement circuit



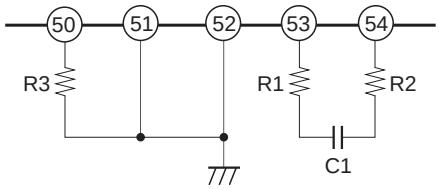
(e) Jitter characteristics measurement circuit

Notes on Operation

1. Clock synthesizer (PLL)

The CXB1582Q has a built-in PLL-based clock recovery circuit which recovers the clock from the serial data. This clock recovery circuit requires an external loop filter and an external resistor which determines the VCO center frequency. The external part circuit and recommended constant values are shown in the figure below.

The parasitic capacitance attached to the IC pins (Pins 50, 53 and 54) which are used to connect external parts should be kept as small as possible in order to obtain the good PLL characteristics. In addition, resistor R3 should have a small temperature coefficient to reduce the temperature dependence of the VCO oscillation frequency.

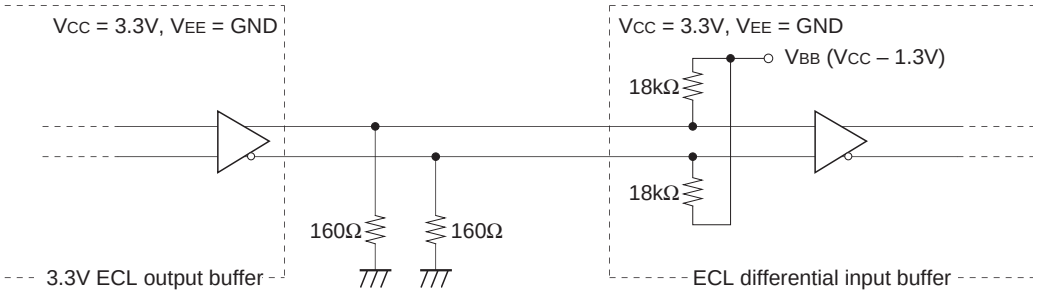


R1: 200Ω
R2: 200Ω
R3: 4.7kΩ
C1: 0.01µF

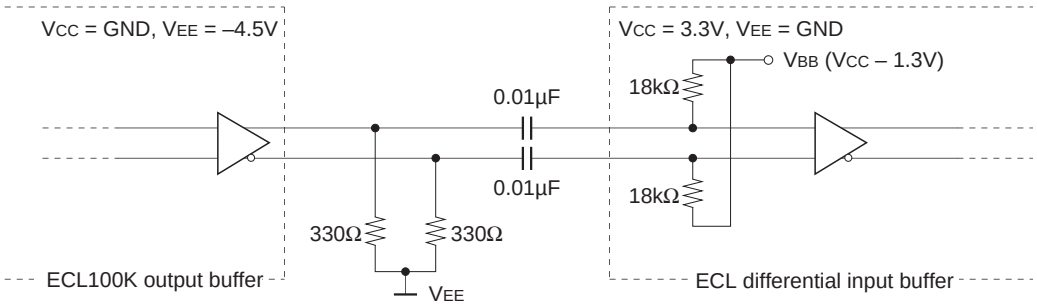
Fig. 1. External Part Circuit and Recommended Constants

2. ECL input circuit

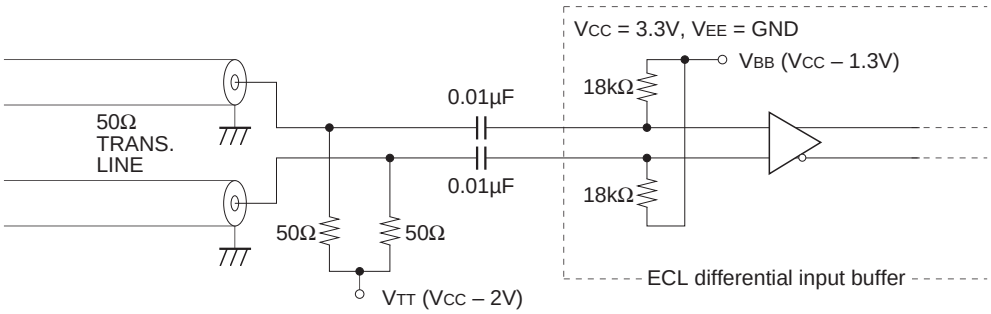
The ECL differential input pins of the CXB1582Q are biased to V_{BB} (Vcc – 1.3V) via an 18kΩ resistor in the IC. See the figures below for ECL differential input methods.



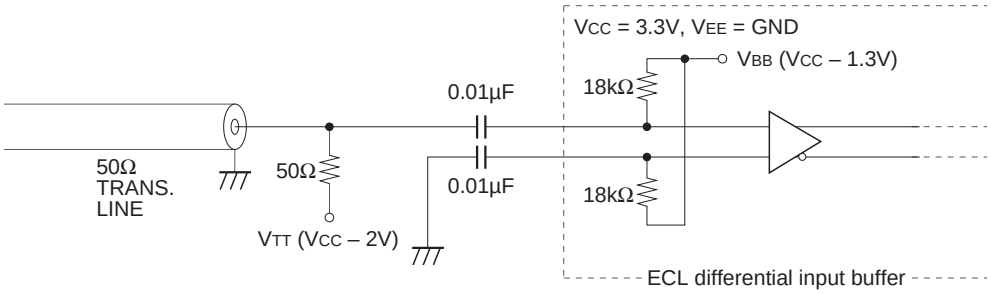
(a) ECL differential signal from 3.3V ECL output buffer



(b) ECL differential signal from ECL100K output buffer



(c) ECL differential signal from 50Ω transmission line

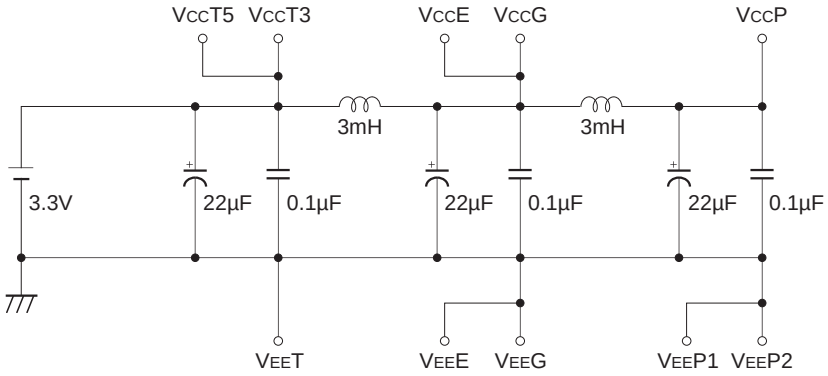


(d) ECL single signal from 50Ω transmission line

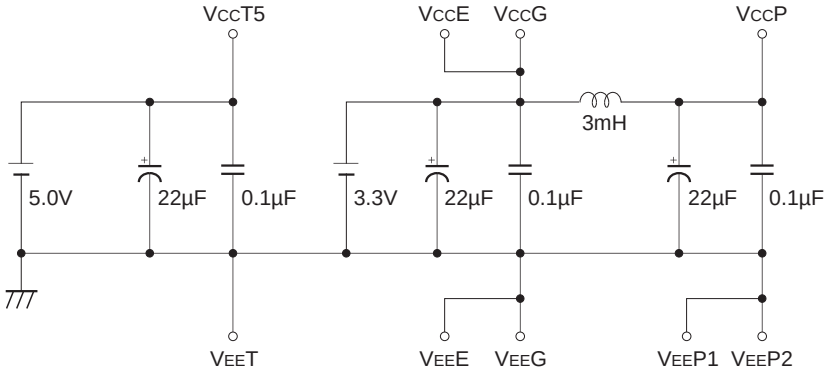
Fig. 2. ECL Input Circuits

3. Power supply

Power can be supplied to the CXB1582Q by either a single 3.3V power supply or a dual 3.3V/5V power supply. When a TTL output high level of 2.2V is sufficient (for example, when only interfacing with a 3.3V CMOS), use a single 3.3V power supply. When a TTL output high level of greater than 2.2V is required (for example, when interfacing with a 5V TTL/CMOS), use a dual 3.3V/5V power supply.



(a) Single 3.3V power supply



(b) Dual 3.3V/5V power supply

Fig. 3. Power Supply Circuits

4. Power-on reset signal (POR*)

The CXB1582Q has a power-on reset signal output (POR*). As shown in figure (a) below, this signal is output at low level for approximately 100ns after the power is turned on, after which it goes to high level and can be used as the system reset signal. The low level time Tpor can be adjusted by capacitance Crt connected to the RTCAP pin as shown in figure (b) below. Tpor conforms roughly to the following equation.

$$Tpor = 90ns \times (1 + Crt/10pf)$$

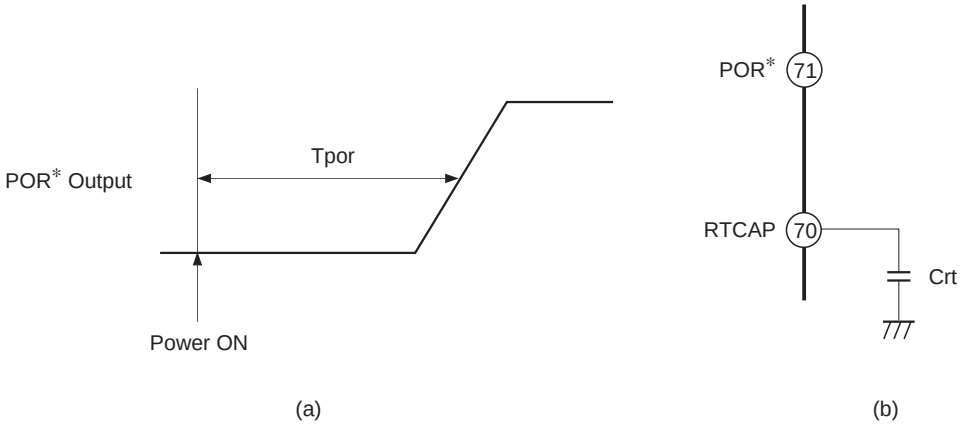
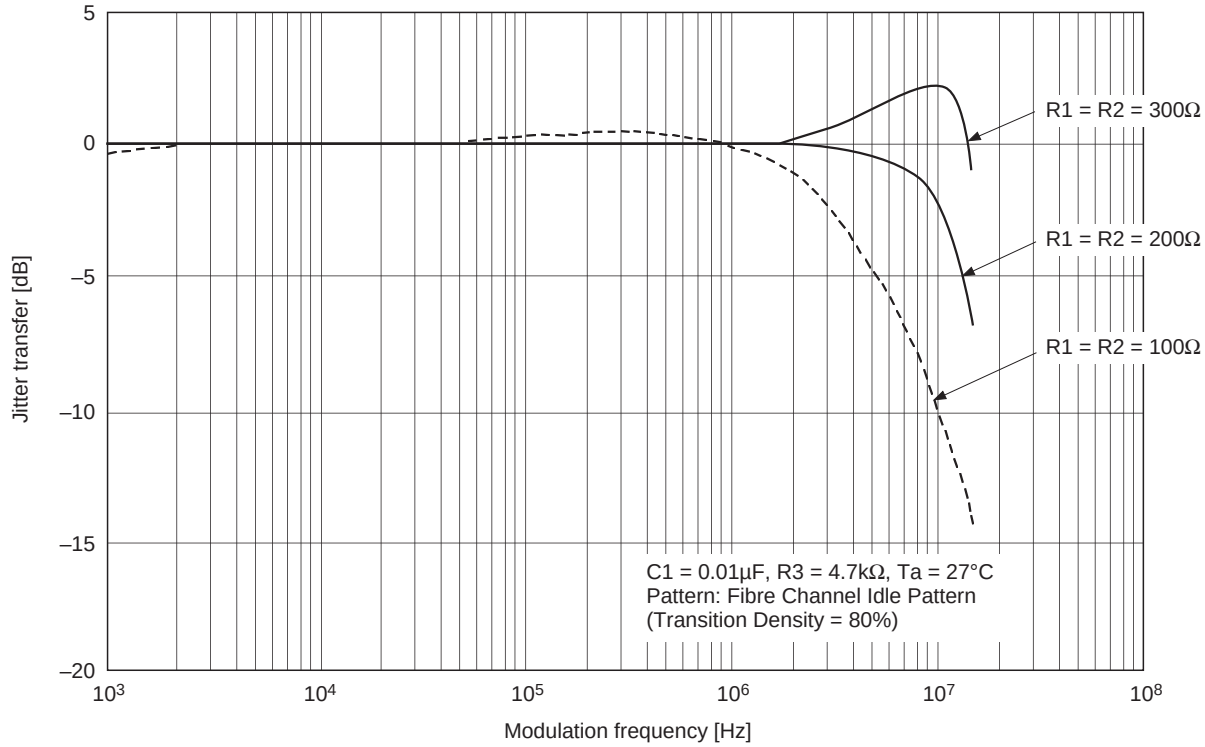


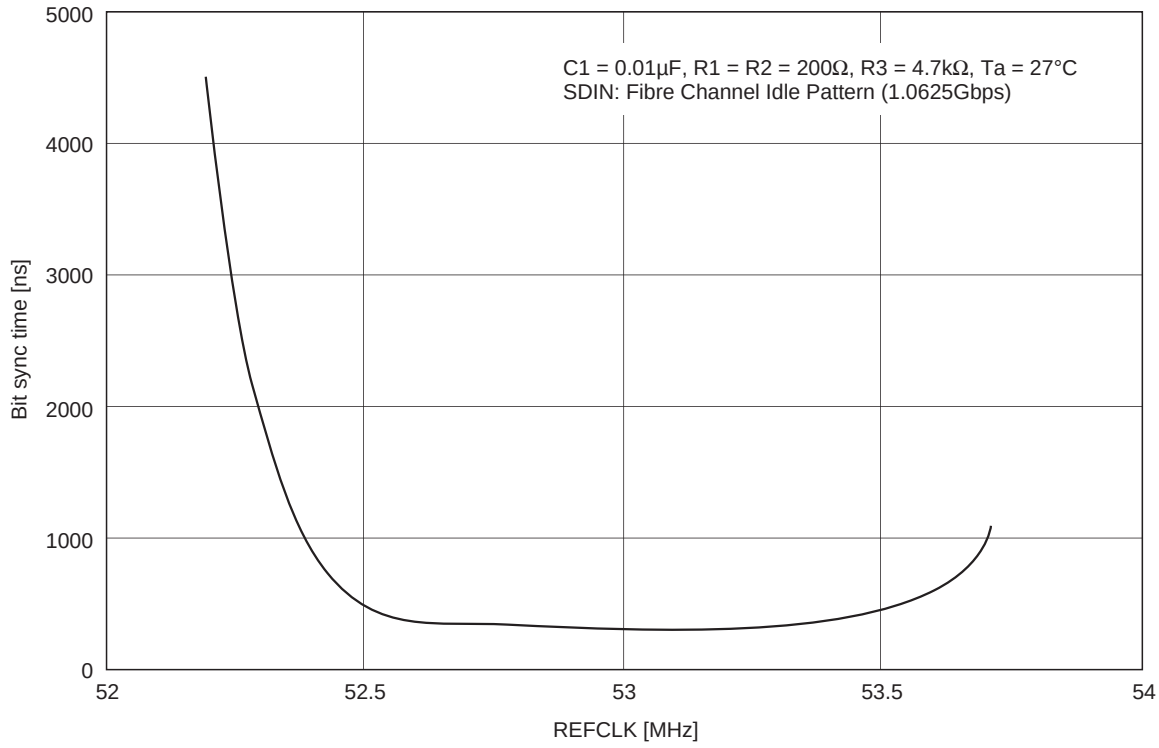
Fig. 4. Power-on Reset Signal Setting

Example of Representative Characteristics

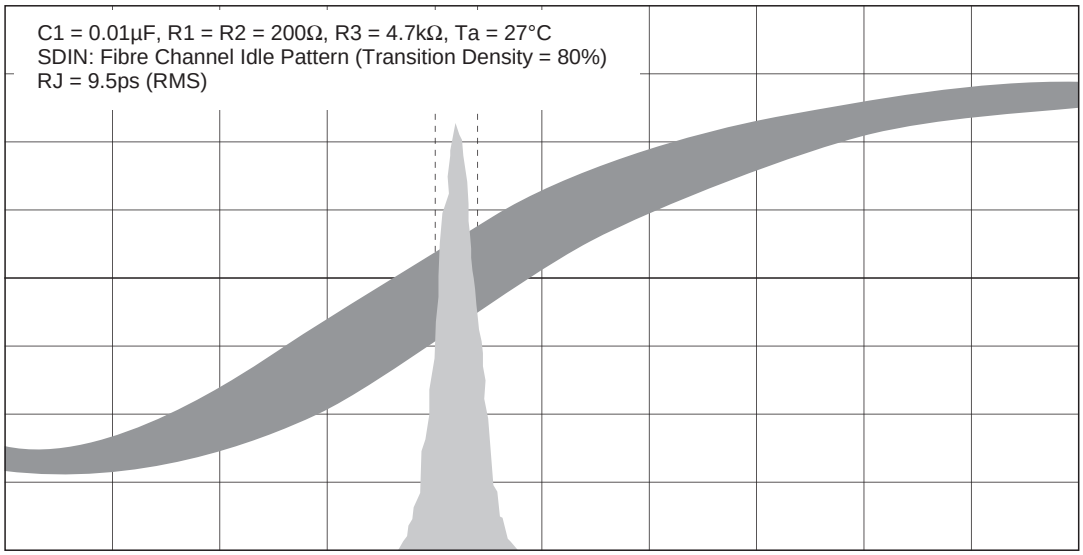
Jitter transfer (1.0625GHz operation)



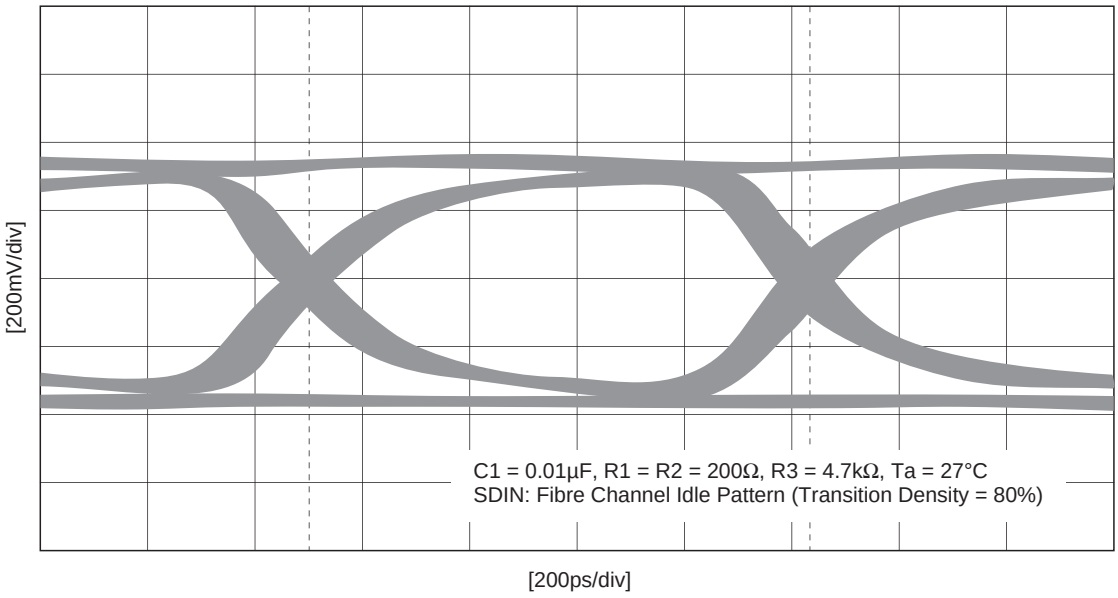
Bit sync time (1.0625GHz operation)



Example of RJ measurement (recovery clock, 1.0625GHz operation)

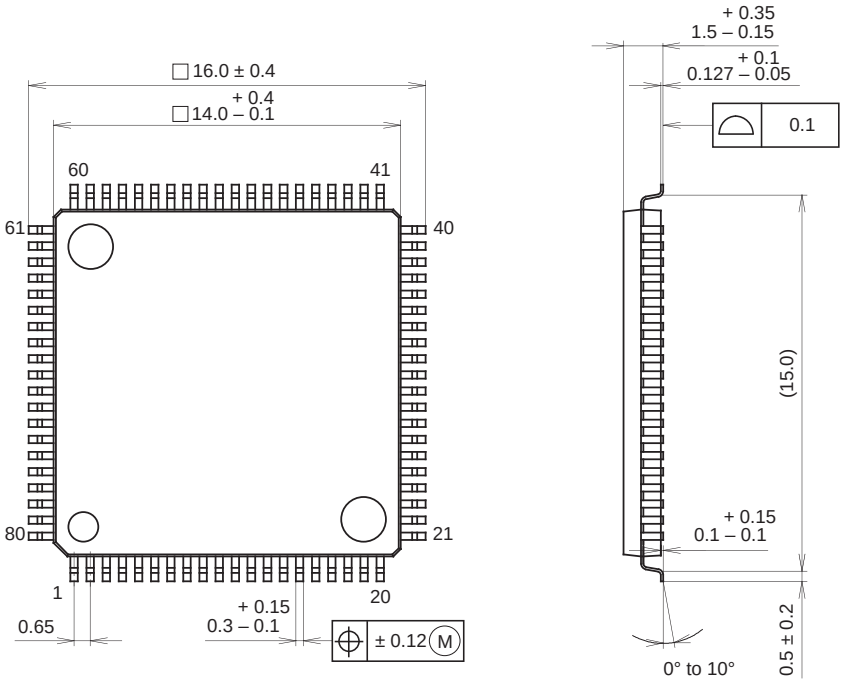


Eye pattern (retimed data, 1.0625GHz operation)



Package Outline Unit: mm

80PIN QFP (PLASTIC)



SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.6g